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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,099	KAWAHARA ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29* is/are allowed.

6)☒ Claim(s) *15-18 and 20-28* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated May 22, 2006.

2. Claims 15-29 are presented for examination. Applicant has canceled claims 1-14.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Datar et al., US Patent 6625740, hereinafter Datar.

4. In re claim 15, Datar discloses a semiconductor device [system on chip 400] comprising:

- A functional circuit block [201] for performing a processing when an instruction or data is inputted [col.7, ll.1-10].
- A power status control circuit [401; dedicated power control circuit] for controlling a power status of said functional circuit block [col.5, ll.43-54].
- A prediction circuit [401] coupled to receive the instruction [*dynamic* power control codes implemented as separate instructions] or data for controlling said power status control circuit, independently of other computation devices, based on said instruction or data [col.5, l.55 – col.6, l.14; prediction circuit retrieves instructions from memory and independently determines activation/deactivation of functional circuit blocks] and on an interval between successive instructions or data [col.6, ll.15-31; look ahead over interval of clock cycles after execution of instruction to predict whether block would need to be

powered] which are inputted to both the functional circuit block and the prediction circuit [fig.4; col.4, l.58 – col.5, l.5; col.7, ll.1-10; 401 accesses instructions from 207 via dedicated line; 201 accesses instructions from 207 via 206].

5. As to claim 16, Datar discloses, wherein said prediction circuit has a function to control said functional circuit block to process said instruction or data inputted into said functional circuit block [col.6, ll.4-14; enable blocks for processing].

6. As to claim 17, Datar discloses:

- Wherein said power status control circuit comprises at least a power shutdown circuit, or an operating voltage setting circuit, and/or an operating frequency setting circuit [col.6, ll.58-67; zero frequency at sleep mode].
- Wherein clock pulses are inputted into said functional circuit block and said power status control circuit [inherently, digital systems require clock pulses to operate for synchronization and timing purposes].
- Wherein, when there is an input to said functional circuit block, said power shutdown circuit supplies a power to said functional circuit block, said operating voltage setting circuit sets an operating voltage supplied to said functional circuit blocks to a first voltage, and said operating frequency setting circuit set an operating frequency of said functional circuit block to a first frequency [col5, l.43 – col.6, l.67; enabling circuit block inherently requires setting various attributes in the broadest interpretation].
- Wherein, when there is no input to said functional circuit block for a period in which said power status control circuit counts said clock pulses n times, said power shutdown circuit shuts down a power supplied to said functional circuit block, said operating voltage

setting circuit sets said operating voltage supplied to said functional circuit block to a second voltage lower than said first voltage, and said operating frequency setting circuit sets said operating frequency of said functional circuit block to a second frequency lower than said first frequency [col.5, l.43 – col.6, l.67; auto timers disabling circuit blocks after elapsed time of no activity].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Datar as applied to claim 15 above, and further in view of Dean et al., US Patent 6477654, hereinafter Dean.

9. Datar taught each and every limitation of the claim, as discussed above in reference to claim 15. In particular, Datar discloses:

- Wherein said power status control circuit comprises a power shutdown circuit [inherently, a power shutdown circuit in the broadest interpretation is needed to switch on/off blocks] for shutting down power which is supplied to said functional circuit block, said power shutdown circuit being coupled to said functional circuit block and a power supply [119] [col.6, ll.58-67].
- Wherein clock pulses are inputted into said functional circuit block and said power status control circuit [inherently, digital systems require clock pulses to operate for synchronization and timing purposes].

- Wherein said prediction circuit comprises a counter [auto timer] for counting the number of clock pulses inputted to said functional circuit block and to said counter, a control circuit [inherently, a control circuit in the broadest interpretation is needed to control the power shutdown circuit] for controlling said power shutdown circuit, and an input detection circuit receiving the instruction or data inputted to said functional circuit block for detecting said instruction or data inputted to said functional circuit block [col.7, ll.1-10; inherently, an input detection circuit in the broadest interpretation is needed at 401 to detect instructions retrieved from 207 in order to latch the instructions properly for 401 to make appropriate power control determinations; same instructions are retrieved separately as 401 and 201 are separate yet have to operate in synch according to instructions] [col.4, l.58 – col.5, l.5; col.5, l.55 – col.6, l.14; col.6, ll.58-67].
- Wherein said counter outputs a first signal to said control circuit when a number of said clocks pulses counted is n [elapsed time] [col.6, ll.58-67].

10. Datar did not discuss the operational details of the counter and associated circuits.

11. Dean discloses a semiconductor device [integrated circuit]:

- Wherein a counter [183] outputs a first signal [expire output] to a control circuit [184] when a number of said clock pulses counted is n [col.6, ll.1-9].
- Wherein, when there is no instruction or data inputted to the functional circuit block [182], an input detection circuit [12] outputs a reset signal to said counter to reset a counting of said clock pulse and outputs a second signal [reset] to said control circuit, and said control circuit outputs an output signal of a first state to shut down said power

supplied to said functional circuit block when both said first [expire] and second [reset] signals are inputted to said control circuit [col.5, l.60 – col.6, l.45].

12. It would have been obvious to one of ordinary skill in the art, having the teachings of Datar and Dean before him at the time the invention was made, to modify the semiconductor device taught by Datar to include the teachings of Dean, in order to obtain the semiconductor device wherein, when there is no instruction or data inputted to the functional circuit block, an input detection circuit outputs a reset signal to said counter to reset a counting of said clock pulse and outputs a second signal to said control circuit, and said control circuit outputs an output signal of a first state to shut down said power supplied to said functional circuit block when both said first and second signals are inputted to said control circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to minimize power consumption in a system with multiple functional blocks [Dean: col.1, l.51 – col.2, l.24].

13. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datar as applied to claim 15 above, and further in view of Dean and Ranta-aho et al., US Patent 6353308, hereinafter Ranta.

14. In re claim 20, Datar discloses each and every limitation of the claim as discussed above in reference to claim 15. In particular, Datar discloses, wherein clock pulses are inputted into said functional circuit block [inherently, digital systems require clock pulses to operate for synchronization and timing purposes], said power status control circuit block comprises an operation voltage setting circuit for setting an operating voltage of said functional circuit block, said operation voltage setting circuit being coupled to said functional circuit block and a power supply [col.6, ll.58-67]. Datar did not discuss the details of the prediction circuit.

15. Dean discloses a semiconductor device [integrated circuit]:

- Wherein a prediction circuit [22, 12, 110, 118, 183, 184, and other associated circuitries] comprises a switch [184] provided between a control signal line and an operating voltage setting circuit [181], the control signal line supplying a first and second signal voltage to the operating voltage setting circuit [1 or 0], and a switch control circuit [12, 110, 118, 183, and other associated circuitries] inputted with the instruction or data and the clock pulses and controlling the switch [fig.2].
- Wherein, when the data or instruction is inputted to a functional circuit block [182], the switch control circuit controls the switch to supply the first signal voltage to the operating voltage setting circuit, and when the switch control circuit counts the clock n times [expire output] after the data or instruction is inputted to the functional circuit block, the switch control circuit controls the switch to supply the second signal voltage to the operating voltage setting circuit [col.5, l.60 – col.6, l.45].

16. It would have been obvious to one of ordinary skill in the art, having the teachings of Datar and Dean before him at the time the invention was made, to modify the semiconductor device taught by Datar to include the teachings of Dean, in order to obtain the semiconductor device with the limitations discussed above. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to minimize power consumption in a system with multiple functional blocks [Dean: col.1, l.51 – col.2, l.24].

17. Datar and Dean did not disclose separate control signal lines for the first and second signal voltages.

18. Ranta discloses a semiconductor device [1], wherein a circuit comprises a first control signal line [18] supplying a first signal voltage and a second control signal [19] line supplying a second voltage lower than the first signal voltage [col.6, ll.21-28].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Ranta, Datar and Dean before him at the time the invention was made, to modify the semiconductor device taught by Datar and Dean to include the teachings of Ranta in order to obtain the claimed semiconductor device, as the separate control signal lines taught by Ranta is very well known in the art and suitable for use with the semiconductor device of Datar and Dean. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to minimize power consumption [Ranta: col.1, l.4 – col.2, l.33].

20. As to claim 21, Datar discloses, wherein said function circuit block [201] comprises a register [205] for temporarily storing said instruction or data and functional block [e.g., 202] for computation, and Dean discloses, wherein said switch control circuit [184] controls said register [182 analogous to Datar 201] in accordance with said instruction or data inputted [related to set/reset] to said functional circuit block and said number of clock pulses counted [expire output] [col.5, l.32 – col.6, l.45].

21. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datar as applied to claim 15 above, and further in view of Kataoka et al., US Patent 5602975, hereinafter Kataoka.

22. In re claim 22, Datar discloses each and every limitation of the claim as discussed above in reference to claim 15. In particular, Datar discloses:

- Wherein the power status control circuit comprises an operating frequency setting circuit [inherently, an operating frequency setting circuit in the broadest interpretation is needed to set the clock to active or sleep mode frequency] outputting clock pulses to the functional circuit block [col.6, ll.58-67].
- Wherein the prediction circuit comprises an input detection/clock counting circuit [401 including the auto timer] receiving said instruction or data and detecting the instruction or data which is inputted to the functional circuit block [col.7, ll.1-10; detect instructions received from 207 in order to latch the instructions properly for 401 to make appropriate power control determinations; same instructions are retrieved separately as 401 and 201 are separate yet have to operate in synch according to instructions], counting a number of clock pulses inputted to the input detection/clock counting circuit and controlling the operating frequency setting circuit, and a setting register for storing a number of the clock pulses [inherently, a register in the broadest interpretation is needed to keep count for the timer] [col.5, l.55 – col.6, l.14; col.6, ll.58-67].
- Wherein, when the instruction or data is inputted to the functional circuit block, the input detection/clock counting circuit controls the operating frequency setting circuit to output clock pulses of a first frequency [active mode] [col.5, l.55 – col.6, l.14; col.6, ll.58-67].
- Wherein, when said input detection/clock counting circuit counts the number n of clock pulses after the instruction or data is not inputted to the functional circuit block, the input/detection/clock counting circuit controls the operating frequency setting circuit to output clock pulses of a second frequency [sleep mode] [col.5, l.55 – col.6, l.14; col.6, ll.58-67].

23. Datar did not discuss details of the operating frequency setting circuit.

24. Kataoka discloses a semiconductor device [fig.1] comprising:

- An operating frequency setting circuit having a frequency divider [12], the frequency divider being able to vary a frequency dividing ratio [factor] [col.5, ll.52-67].
- Wherein the operating frequency setting circuit outputs clock pulses of a lower frequency by increasing the frequency dividing ratio of the frequency divider [col.5, ll.52-67].

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Datar and Kataoka before him at the time the invention was made, to modify the semiconductor device taught by Datar to include the frequency divider taught by Kataoka in order to obtain the claimed semiconductor device, as the frequency divider taught by Kataoka is very well known in the art and suitable for use with the semiconductor device of Datar. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to minimize power consumption [Kataoka: col.5, l.52 – col.6, l.6].

26. As to claim 23, Datar discloses:

- Wherein said function circuit block [201] comprises a register [205] for temporarily storing said instruction or data and functional block [e.g., 202] for computation.
- Wherein said input detection/clock counting circuit controls said register in accordance with said instruction or data and the number of clock pulses [col.5, l.32 – col.6, l.45; col.6, ll.58-67].

27. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datar as applied to claim 17 above, and further in view of Brouwer., US Patent 6760303.

28. Datar discloses each and every limitation of the claim as discussed above in reference to claim 17. In particular, Datar discloses the power status control circuit counts n in accordance with a history [col.6, ll.15-31; a history in the broadest interpretation is needed in order to plan the timely enabling and disabling of blocks]. Datar did not disclose explicitly a circuit for updating the number n of clock pulses.

29. Brouwer discloses a semiconductor device [26] comprising a circuit for updating the number n of clock pulses [timeout value T] [col.12, l.49 – col.13, l.8].

30. It would have been obvious to one of ordinary skill in the art, having the teachings of Datar and Brouwer before him at the time the invention was made, to modify the semiconductor device taught by Datar to include the teachings of Brouwer in order to obtain the claimed semiconductor device, as the updating the number n of clock pulses taught by Brouwer is very well known in the art and suitable for use with the semiconductor device of Datar. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to adapt to system changes [Brouwer: col. 12, l.49 – col.13, l.8].

31. As to claim 25, Examiner hereby takes Official Notice that it is well known in the art to use a rewritable nonvolatile semiconductor memory for storing an update result.

32. It would have been obvious to one of ordinary skill in the art to modify the semiconductor device taught by Datar and Brouwer to include the rewritable nonvolatile semiconductor memory in order to store the update result, as the rewritable nonvolatile semiconductor memory is very well known in the art and suitable for use with the semiconductor device of Datar and Brouwer. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to store an update result.

33. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Datar as applied to claim 15 above, and further in view of Mohamed et al., US Patent 6014512, hereinafter Mohamed.

34. Datar discloses each and every limitation of the claim as discussed above in reference to claim 15. In particular, Datar discloses the semiconductor device comprising a central processing unit [101] that outputs a control signal to the power status control circuit for controlling the power status control circuit and outputs the instruction or data which is inputted to the functional circuit block [col.2, ll.46-57; col.4, ll.23-34; central processing unit provides overall system management]. Datar did not disclose a power control table.

35. Mohamed discloses a central processing unit [to run simulator] comprising a power control table [clock cycle lookup table] [col.8, ll.36-67].

36. It would have been obvious to one of ordinary skill in the art, having the teachings of Datar and Mohamed before him at the time the invention was made, to modify the semiconductor device taught by Datar to include the power control table of Mohamed, in order to obtain the semiconductor device comprising a central processing unit comprising a power control table, wherein the central processing unit outputs a control signal to the power status control circuit for controlling the power status control circuit by referring to the power control table and outputs the instruction or data which is inputted to the functional circuit block. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce clock comparisons in a system with multiple blocks [Mohamed: col.8, ll. 14-67].

37. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datar and Mohamed as applied to claim 26 above, and further in view of Takayama, Japanese Patent 408295065A.

38. In re claim 27, Datar and Mohamed disclose each and every limitation of the claim as discussed above in reference to claim 26. In particular, Datar discloses a decoder for decoding instruction or data and outputting the control signal [enable or disable] based on the instruction or data [col.5, l.55 – col.6, l.14]. Datar and Mohamed did not disclose explicitly a second instruction or data which is externally inputted.

39. Takayama discloses a central processing unit [19 with associated circuitries] comprising a decoder [inherently, a decoder in the broadest interpretation is needed to process the external job command] for decoding an instruction or data [job command] which is externally inputted to the central processing unit, the central processing unit outputting the control signal [on/off] based on the instruction or data [constitution].

40. It would have been obvious to one of ordinary skill in the art, having the teachings of Takayama, Datar and Mohamed before him at the time the invention was made, to modify the semiconductor device taught by Datar and Mohamed to include the teachings of Takayama, in order to obtain the claimed semiconductor device, as the external second instruction or data taught by Takayama is very well known in the art and suitable for use with the semiconductor device of Datar and Mohamed. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption in a system with multiple blocks [Takayama: purpose].

41. As to claim 28, Takayama discloses, a plurality of functional circuit blocks and wherein the power status of each of the plurality of function circuit block is controlled by the control signal outputted by the central processing unit [19 with associated circuitries], which control signal is obtained by the decoding of the second instruction or data power controlling information by using the decoder [constitution].

Allowable Subject Matter

42. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

43. Claim 29 is allowed.

Response to Arguments

44. Applicant's arguments dated May 22, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER
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Tse Chen
May 31, 2006